M-8880 DTMF Transceiver

Advanced CMOS technology for low power consumption and increased noise immunity

Complete DTMF transmitter/receiver in a single chip

Standard 6500/6800 series microprocessor port

Central office quality and performance

Adjustable guard time

Automatic tone burst mode

Call progress mode

Single +5 Volt power supply

20-pin DIP and SOIC packages

2 MHz microprocessor port operation

Inexpensive 3.58 MHz crystal

No continuous 2 clock required, only strobe

Applications include: paging systems, repeater systems/mobile radio, interconnect dialers, PBX systems, computer systems, fax machines, pay telephones, credit card verification

The M-8880 is a complete DTMF Transmitter/Receiver that features adjustable guard time, automatic tone burst mode, call progress mode, and a fully compatible 6500/6800 microprocessor interface. The receiver portion is based on the industry standard M-8870 DTMF Receiver, while the transmitter uses a switched-capacitor digital-to-analog converter for low-distortion, highly accurate DTMF signaling. Tone bursts can be transmitted with precise timing by making use of the automatic tone burst mode. To analyze call progress tones, a call progress filter can be selected by an external microprocessor.

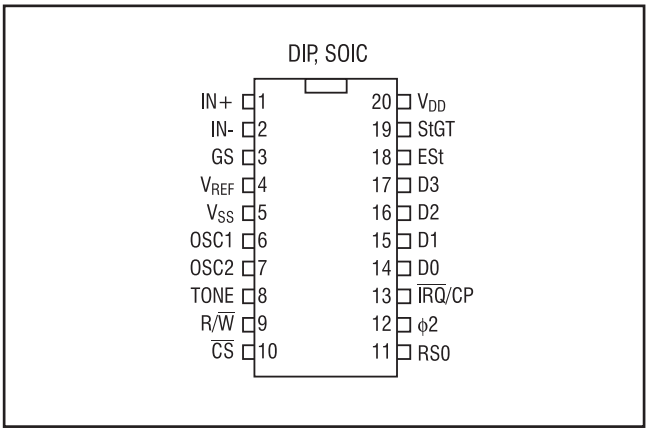


Figure 1 Pin Diagram

Functional Description

M-8880 functions consist of a high-performance DTMF receiver with an internal gain setting amplifier and a DTMF generator that contains a tone burst counter for generating precise tone bursts and pauses. The call progress mode, when selected, allows the detection of call progress tones. A standard 6500/6800 series microprocessor interface allows access to an internal status register, two control registers, and two data registers.

Input Configuration

The input arrangement consists of a differential input operational amplifier and bias sources (V_{REF}) for biasing the amplifier inputs at $V_{DD}/2$. Provisions are made for the connection of a feedback resistor to the op-amp output (GS) for gain adjust-

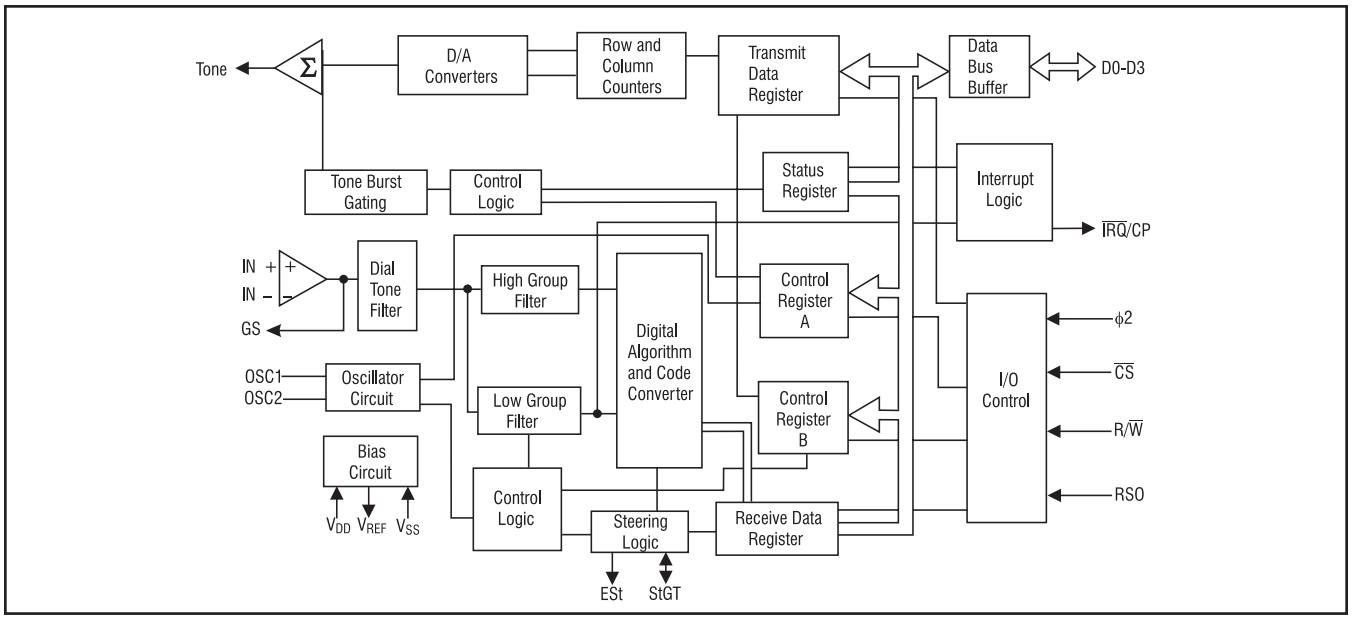


Figure 2 Block Diagram

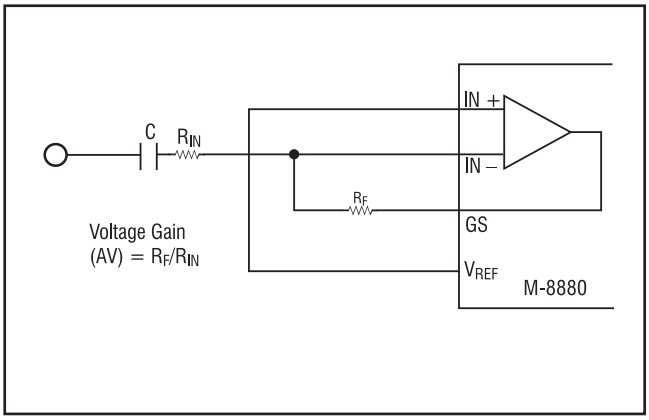


Figure 3 Single-Ended Input Configuration

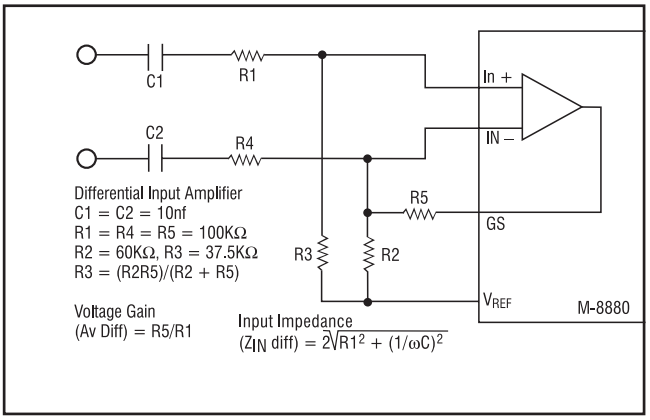


Figure 4 Differential Input Configuration

ment. In a single-ended configuration, the input pins should be connected as shown in Figure 3. Figure 4 shows the necessary connections for a differential input configuration.

Receiver Section

The low and high group tones are separated by applying the DTMF signal to the inputs of two sixth-order switched capacitor bandpass filters with bandwidths that correspond to the low and high group frequencies listed in Table 2. The low group filter incorporates notches at 350 and 440 Hz, providing excellent dial tone rejection. Each filter output is followed by a single-order switched capacitor filter that smooths the signals prior to limiting. Limiting is performed by high-gain comparators with hysteresis to prevent detection of unwanted low-level signals. The comparator outputs provide full-rail logic swings at the incoming DTMF signal frequencies.

A decoder employs digital counting techniques to determine the frequencies of the incoming tones, and to verify that they correspond to standard DTMF frequencies. A complex averaging algorithm protects against tone simulation by extraneous signals (such as voice), while tolerating small deviations in frequency. The algorithm provides an optimum combination of immunity to talkoff with tolerance to interfering frequencies (third tones) and noise. When the detector recognizes the presence of two valid tones (referred to as "signal condition"), the early steering (ESt) output goes to an active state. Any subsequent loss of signal condition will cause ESt to assume an inactive state.

Steering Circuit: Before a decoded tone pair is registered, the receiver checks for a valid signal duration (referred to as "character recognition condition"). This check is performed by an external RC time constant driven by ESt. A logic high on ESt

Table 1 Pin Functions

Name	Description
IN+	Noninverting op-amp input.
IN-	Inverting op-amp input.
GS	Gain select. Gives access to output of front end differential amplifier for connection of feedback resistor.
V_{REF}	Reference voltage output. Nominally $V_{DD}/2$ is used to bias inputs at mid-rail.
V_{SS}	Negative power supply input.
OSC1	DTMF clock/oscillator input.
OSC2	Clock output. A 3.5795 MHz crystal connected between OSC1 and OSC2 completes the internal oscillator circuit.
TONE	Dual tone multifrequency (DTMF) output.
R/$\overline{W}$	Read/write input. Controls the direction of data transfer to and from the microprocessor and the receiver/transmitter. TTL compatible.
$\overline{CS}$	Chip select. TTL input ($\overline{CS}$ = 0 to select the chip).
RS0	Register select input. See Table 6. TTL compatible.
ϕ2	System clock input. May be continuous or strobed only during read or write. TTL compatible.
$\overline{IRQ}$/CP	Interrupt request to microprocessor (open-drain output). Also, when call progress (CP) mode has been selected and interrupt enabled, the IRQ/CP pin will output a rectangular wave signal representative of the input signal applied at the input op-amp. The input signal must be within the bandwidth limits of the call progress filter. See Figure 11
D0 - D3	Microprocessor data bus. TTL compatible.
ESt	Early steering output. Presents a logic high once the digital algorithm has detected a valid tone pair (signal condition). Any momentary loss of signal condition will cause ESt to return to a logic low.
St/GT	Steering input/guard time output (bidirectional). A voltage greater than V_{TSt} detected at St causes the device to register the detected tone pair and update the output latch. A voltage less than V_{TSt} frees the device to accept a new tone pair. The GT output acts to reset the external steering time-constant; its state is a funciton of ESt and the voltage on St.
V_{DD}	Positive power supply input.

causes V_C (see Figure 5) to rise as the capacitor discharges. Provided that the signal condition is maintained (ESt remains high) for the validation period (t_{GTP}), V_C reaches the threshold (V_{TSt}) of the steering logic to register the tone pair, latching its corresponding 4-bit code (see Table 2) into the receive data register.

Table 2 Tone Encoding/Decoding

F_{LOW}	F_{HIGH}	Digit	D3	D2	D1	D0
697	1209	1	0	0	0	1
697	1336	2	0	0	1	0
697	1477	3	0	0	1	1
770	1209	4	0	1	0	0
770	1336	5	0	1	0	1
770	1477	6	0	1	1	0
852	1209	7	0	1	1	1
852	1336	8	1	0	0	0
852	1477	9	1	0	0	1
941	1336	0	1	0	1	0
941	1209	*	1	0	1	1
941	1477	#	1	1	0	0
697	1633	A	1	1	0	1
770	1633	B	1	1	1	0
852	1633	C	1	1	1	1
941	1633	D	0	0	0	0
0 = logic low, 1 = logic high						

At this point the StGT output is activated and drives V_C to V_{DD}. StGT continues to drive high as long as ESt remains high. Finally, after a short delay to allow the output latch to settle, the delayed steering output flag goes high, signaling that a received tone pair has been registered. It is possible to monitor the status of the delayed steering flag by checking the appropriate bit in the status register. If interrupt mode has been selected, the $\overline{IRQ}$/CP pin will pull low when the delayed steering flag is active.

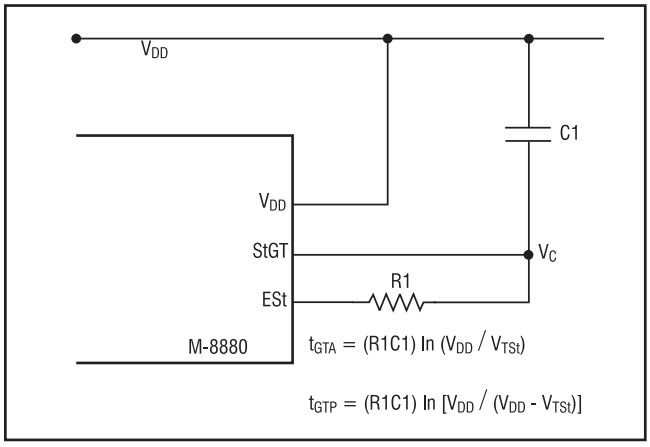


Figure 5 Basic Steering Circuit

The contents of the output latch are updated on an active delayed steering transition. This data is presented to the 4-bit bidirectional data bus when the receive data register is read.

The steering circuit works in reverse to validate the interdigit pause between signals. Thus, as well as rejecting signals too short to be considered valid, the receiver will tolerate signal interruptions (dropout) too short to be considered a valid pause. This capability, together with the ability to select the steering time constants externally, allows the designer to tailor performance to meet a wide variety of system requirements.

Guard Time Adjustment: The simple steering circuit shown in Figure 5 is adequate for most applications. Component values are chosen according to the formula:

$$t_{REC} = t_{DP} + t_{GTP}$$
$$T_{ID} = t_{DA} + t_{GTA}$$

The value of t_{DP} is a device parameter and t_{REC} is the minimum signal duration to be recognized by the receiver. A value for C1 of 0.1 µF is recommended for most applications, leaving R1 to be selected by the designer. Different steering arrangements may be used to select independently the guard times for tone present (t_{GTP}) and tone absent (t_{GTA}). This may be necessary to meet system specifications that place both accept and reject limits on both tone duration and interdigit pause. Guard time adjustment also allows the designer to tailor system parameters such as talkoff and noise immunity. Increasing t_{REC} improves talkoff performance since it reduces the probability that tones simulated by speech will maintain signal condition long enough to be registered. Alternatively, a relatively short t_{REC} with a long t_{DO} would be appropriate for extremely noisy environments where fast acquisition time and immunity to tone dropouts are required. Design information for guard time adjustment is shown in Figure 6.

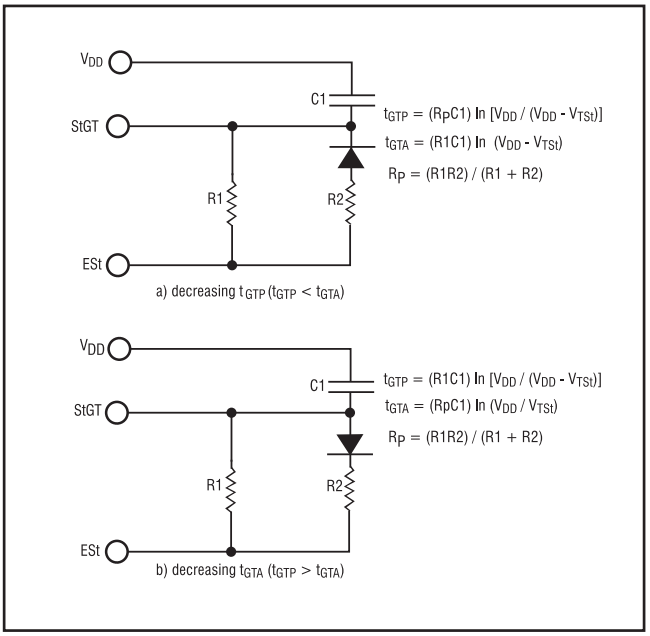


Figure 6 Guard Time Adjustment

Call Progress Filter

A call progress (CP) mode can be selected, allowing the detection of various tones that identify the progress of a telephone call on the network. The call progress tone input and DTMF input are common; however, call progress tones can only be detected when the CP mode has been selected. DTMF signals cannot be

detected if the CP mode has been selected (see Table 3). Figure 7 indicates the useful detect bandwidth of the call progress filter. Frequencies presented to the input (IN+ and IN-) that are within the "accept" bandwidth limits of the filter are hard-limited by a high-gain comparator with the $\overline{IRQ}$ /CP pin serving as the output. The square wave output obtained from the schmitt trigger can be analyzed by a microprocessor or counter arrangement to determine the nature of the call progress tone being detected. Frequencies in the "reject" area will not be detected, and consequently there will be no activity on $\overline{IRQ}$ /CP as a result of these frequencies.

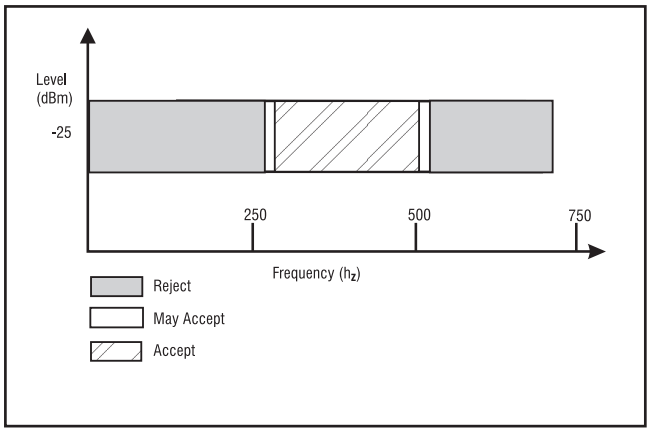


Figure 7 Call Progress Response

DTMF Generator

The DTMF transmitter used in the M-8880 is capable of generating all 16 standard DTMF tone pairs with low distortion and high accuracy. All frequencies are derived from an external 3.58 MHz crystal. The sinusoidal waveforms for the individual tones are digitally synthesized using row and column programmable dividers and switched capacitor digital-to-analog converters. The row and column tones are mixed and filtered, providing a DTMF signal with low total harmonic distortion and high accuracy. To specify a DTMF signal, data conforming to the encoding format shown in Table 2 must be written to the transmit data register. Note that this is the same as the receiver output code. The individual tones that are generated (f_{LOW} and f_{HIGH}) are referred to as low-group and high-group tones. Typically, the high-group to low-group amplitude ratio (twist) is 2 dB to compensate for high-group attenuation on long loops.

Operation: During write operations to the transmit data register, 4-bit data on the bus is latched and converted to a 2 of 8 code for use by the programmable divider circuitry to specify a time segment length that will ultimately determine the tone frequency. The number of time segments is fixed at 32, but the frequency is varied by varying the segment length. When the divider reaches the appropriate count as determined by the input code, a reset pulse is issued and the counter starts again. The divider output clocks another counter that addresses the sinewave lookup ROM. The lookup table contains codes used by the switched capacitor D/A converter to obtain discrete and highly accurate DC voltage levels. Two identical circuits are used to produce row and column tones, which are then mixed using a low-noise summing amplifier. The oscillator described needs no "startup" time as in other DTMF generators, since the crystal oscillator is running continuously, thus providing a high degree of tone burst accuracy. When there is no tone output signal, the TONE pin assumes a DC level of 2.5 volts (typically). A bandwidth limiting filter is incorporated to attenuate distortion products above 4 KHz.

Burst Mode: Certain telephony applications require that generated DTMF signals be of a specific duration, determined either by the application or by any of the existing exchange transmitter specifications. Standard DTMF signal timing can be accomplished by making use of the burst mode. The transmitter is capable of issuing symmetric bursts/pauses of predetermined duration. This burst/pause duration is 51 ms $\pm$ 1 ms, a standard interval for autodialer and central office applications. After the burst/pause has been issued, the appropriate bit is set in the status register, indicating that the transmitter is ready for more data.

The timing described is available when the DTMF mode has been selected. However, when call progress (CP) mode is selected, a secondary burst/pause time is available that extends this interval to 102 ms $\pm$ 2 ms. The extended interval is useful when precise tone bursts of longer than 51 ms duration and 51 ms pause are desired. Note that when CP mode and burst mode have been selected, DTMF tones may be transmitted only and *not* received. In applications requiring a nonstandard burst/pause time, use a software timing loop or external timer. This provides the timing pulses when the burst mode is disabled by enabling and disabling the transmitter.

The M-8880 is initialized on powerup sequence with DTMF mode and burst mode selected.

Single-Tone Generation: A single-tone mode is available whereby individual tones from the low group or high group can be generated. This mode can be used for DTMF test equipment applications, acknowledgment tone generation, and distortion measurements. Refer to Table 4 for details.

Distortion Calculations: The M-8880 is capable of producing precise tone bursts with minimal error in frequency (see Table 3). The internal summing amplifier is followed by a first-order low-pass switched capacitor filter to minimize harmonic components and intermodulation products. The total harmonic distortion for a *single* tone can be calculated using Equation 1, (see Figure 9) which is the ratio of the total power of all the extraneous frequencies to the power of the fundamental frequency expressed as a percentage. The Fourier components of the tone output correspond to V2f... Vnf as measured on the output waveform. The total harmonic distortion for a *dual* tone can be calculated using Equation 2 (see Figure 9).

Table 3 Actual Frequencies vs. Standard Requirements

Active Cell	Output Frequency (Hz) Specified	Actual	% Error
L1	697	699.1	+ 0.30
L2	770	766.2	- 0.49
L3	852	847.4	- 0.54
L4	941	948.0	+ 0.74
H1	1209	1215.9	+ 0.57
H2	1336	1331.7	- 0.32
H3	1447	1471.9	- 0.35
H4	1633	1645.0	+ 0.73

Table 4 Control Register A Description

Bit	Name	Function	Description
b0	TOUT	Tone output	A logic 1 enables the tone output. This function can be implemented in either the burst mode or nonburst mode.
b1	CP/$\overline{\text{DTMF}}$	Mode control	In DTMF mode (logic 0), the device is capable of generating and receiving DTMF signals. When the call progress (CP) mode is selected (logic 1), a 6th-order bandpass filter is enabled to allow call progress tones to be detected. Call progress tones within the specified bandwidth will be presented at the IRQ/CP pin in rectangular wave format if the IRQ bit has been enabled (b2 =1). Also, when the CP mode and burst mode have both been selected, the transmitter will issue DTMF signals with a burst and pause of 102 ms (typ) duration. This signal duration is twice that obtained from the DTMF transmitter, if DTMF mode had been selected. Note that DTMF signals cannot be decoded when the CP mode has been selected.
b2	IRQ	Interrupt enable	A logic 1 enables the interrupt mode. When this mode is active and the DTMF mode has been selected (b1 = 0), the IRQ/CP pin will pull to a logic 0 condition when either (1) a valid DTMF signal has been received and has been present for the guard time or (2) the transmitter is ready for more data (burst mode only).
b3	RSET	Register select	A logic 1 selects control register B on the next write cycle to the control register address. Subsequent write cycles to the control register are directed back to control register A.

Table 5 Control Register B Description

Bit	Name	Function	Description
b0	$\overline{\text{BURST}}$	Burst mode	A logic 0 enables the burst mode. When this mode is selected, data corresponding to the desired DTMF tone pair can be written to the transmit data register, resulting in a tone burst of a specific duration (see Table 12). Subsequently, a pause of the same duration is induced. Immediately following the pause, the status register is updated indicating that the transmit data register is ready for further instructions, and an interrupt will be generated if the interrupt mode has been enabled. Additionally, if call progress (CP) mode has been enabled, the burst and pause duration is increed by a factor of two. When the burst mode is not selected (logic 1), tone bursts of any desired duration may be generated.
b1	TEST	Test mode	By enabling the test mode (logic 1), the $\overline{\text{IRQ}}$/CP pin will present the delayed steering (inverted) signal from the DTMF receiver. Refer to Figure 11 (b3 waveform) for details concerning the output waveform. DTMF mode must be selected (CRA b1 = 0) before test mode can be implemented.
b2	S/$\overline{\text{D}}$	Single/dual tone generation	A logic 0 will allow DTMF signals to be produced. If single-tone generation is enabled (logic 1), either now or column tones (low or high group) can be generated depending on the state of b3 in control register B.
b3	C/$\overline{\text{R}}$	Column/row tones	When used in conjunction with b2 (above), the transmitter can be made to generate single-row or single-column frequencies. A logic0 will select row frequencies and a logic 1 will select column frequencies.

V_L and V_H correspond to the low-group and high-group amplitude, respectively, and V^2_{IMD} is the sum of all the intermodulation components. The internal switched capacitor filter following the D/A converter keeps distortion products down to a very low level.

DTMF Clock Circuit

The internal clock circuit is completed with the addition of a standard 3.579545 MHz television color burst crystal. A number of M-8880 devices can be connected as shown in Figure 8 using only one crystal.

Microprocessor Interface

The M-8880 uses a microprocessor interface that allows precise control of transmitter and receiver functions. Five internal registers are associated with the microprocessor interface, which can be subdivided into three categories: data transfer, transceiver control, and transceiver status. Two registers are associated with data transfer operations. The receive data, read-only, contains the output code of the last valid DTMF tone pair to be decoded. The data entered in the transmit data register determines which tone pair is to be generated (see Table 2).

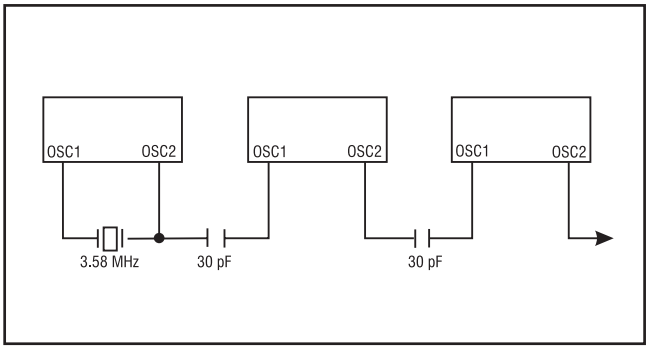


Figure 8 Common Crystal Connection

Data can only be written to the transmit data register. Transceiver control is accomplished with two control registers (CRA and CRB), occupying the same address space. A write operation to CRB can be executed by setting the appropriate bit in CRA. The following write operation to the same address will then be directed to CRB, and subsequent write cycles will then be redirected to CRA. Internal reset circuitry clears the control

registers on powerup; however, as a precautionary measure the initialization software should include a routine to clear the registers. Refer to Tables 3 and 4 for details on the control registers. The $\overline{IRQ}$/CP pin can be programmed to provide an interrupt request signal on validation of DTMF signals, or when the transmitter is ready for more data (burst mode only). The $\overline{IRQ}$/CP pin is configured as an open-drain output device and as such requires a pullup resistor (see Figure 10).

Ordering Information

M-888001P	20-pin plastic DIP
M-8880-01SM	20-pin plastic SOIC
M-8880-01T	20-pin plastic SOIC,Tape and Reel

$$THD(\%) = 100 \frac{\sqrt{V^2 2f + V^2 3f + V^2 4f + \ldots . V^2 nf}}{V_{fundamental}}$$

Equation 1. THD (%) for a Single Tone

$$THD(\%) = 100 \frac{\sqrt{V^2 2L + V^2 3L + ... V^2 nL + V^2 2H + V^2 3H + ... V^2 nH + V^2 IMD}}{\sqrt{V^2 L + V^2 H}}$$

Equation 2. THD (%) for a Dual Tone

Figure 9 Equations

Table 6 Internal Register Functions

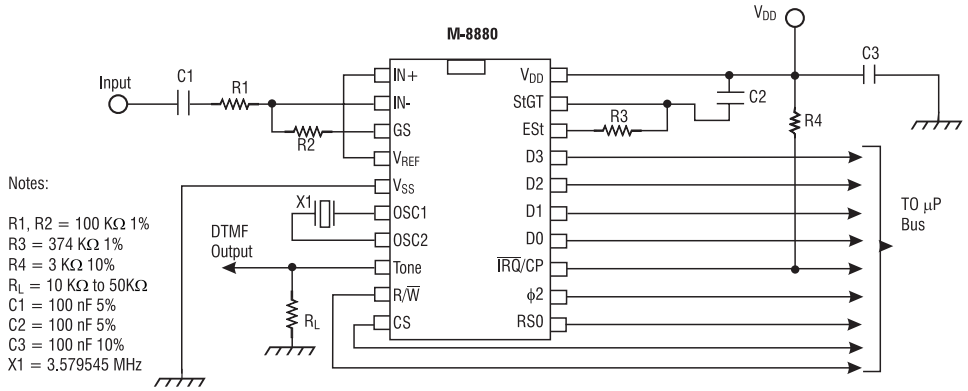
RS0	R/$\overline{W}$	Function
0	0	Write to transmitter
0	1	Read from receiver
1	0	Write to control register
1	1	Read from status register

Table 7 CRA Bit Postions

b3	b2	b1	b0
RSEL	IRQ	CP/$\overline{DTMF}$	TOUT

Table 8 CRB Bit Positions

b3	b2	b1	b0
C/R	S/D	TEST	BURST



Microprocessor-based systems can inject undesirable noise into the supply rails. M-8880 performance can be optimized by keeping noise on the supply rails to a minimum. The decoupling capacitor (C3) should be connected close to the device and ground loops should be avoided.

Figure 10 Application Circuit (Single-Ended Input)

Table 9 Status Register Description

BIT	Name	Status Flag Set	Status Flag Cleared
b0	IRQ	Interrupt has occurred. Bi tone (b1) and/or bit 2 (b2) is set.	Interrupt is inactive. Cleared after status register is read.
b1	Transmit data register empty (burst mode only)	Pause duration has terminated and transmitter is ready for new data.	Cleared after status register is read or when not in burst mode.
b2	Receive data register full	Valid data is in the receive data register.	Cleared after status register is read.
b3	$\overline{\text{Delayed steering}}$	Set on valid detection of the absence of a DTMF signal.	Cleared on detection of a valid DTMF signal.

Table 10 Absolute Maximum Ratings

Parameter	Symbol	Value
Power supply voltage (V_{DD} - V_{SS})	V_{DD}	+ 6.0 V max
Voltage on any pin	V_{dc}	V_{SS} -0.3 V to V_{DD} + 0.3 V
Current on any pin	I_{DD}	10 mA max
Operating temperature	T_A	-40°C to +85°C
Storage temperature	T_S	-65°C to +150°C
Note: Exceeding these ratings may cause permanent damage. Functional operation under these conditions is not implied.		

Table 11 DC Characteristics

Parameter	Symbol	Min	Typ*	Max	Units
Operating supply voltage	V_{DD}	4.75	5.0	5.25	V
Operating supply current	I_{DD}	—	10	15	mA
Power consumption	P_O	—	50	78.75	mW
Inputs					
High-level input voltage, OSC1	V_{IHO}	3.5	—	—	V
Low-level input voltage, OSC1	V_{ILO}	—	—	1.5	V
Input impedance (@ 1 kHz), IN+, IN-	R_{IN}	—	10	—	MΩ
Steering threshold voltage	V_{TSt}	2.2	2.3	2.5	V
Outputs					
High-level output voltage (no load), OSC2	V_{OHO}	V_{DD} - 0.1V	—	—	V
Low-level output voltage (no load), OSC2	V_{OLO}	—	—	0.1	V
Output leakage current (V_{OH} = 2.4V), IRQ	I_{OZ}	—	1.0	10.0	µA
V_{REF} output voltage (no load)	V_{REF}	2.4	—	2.7	V
V_{REF} output resistance	R_{OR}	—		1.0	kΩ
Data Bus					
Low-level input voltage	V_{IL}	—	—	0.8	V
High-level input voltage	V_{IH}	2.0	—	—	V
Low-level output voltage (I_{OL} = 1.6 mA)	V_{OL}	—	—	0.4	V
High-level output voltage (I_{OH} = 400 µA)	V_{OH}	2.4	—	—	V
Input leakage current (V_{IN} = 0.4 to 2.4 V)	I_{IZ}	—	—	10.0	µA
All voltages referenced to V_{SS} unless otherwise noted. V_{DD} = 5.0 V ± 5%; f_C = 3.579545 MHz; T_A = -40°C to +85°C, unless otherwise noted. *Typical values are for use as design aids only, and are not guaranteed or subject to production testing.					

Table 12 AC Characteristics

PARAMETER	SYMBOL	MIN	TYP*	MAX	UNITS
Receive signal conditions					
Valid input signal levels (each tone of composite signal; Notes 1, 2, 3, 5, 6, 9)		-29 27.5	— —	+1 869	dBm mV_{RMS}
Positive twist accept (Notes 2, 3, 6, 9)		—		6	dB
Negative twist accept (Notes 2, 3, 6, 9)		—		6	dB
Frequency deviation accept (Notes 2, 3, 5, 9)		± 1.5% ± 2 Hz	—	—	Nom.
Frequency deviation reject (Notes 2, 3, 5)		± 3.5%	—	—	Nom.
Third tone tolerance (Notes 2, 3, 4, 5, 9, 10)		—	-16	—	dB
Noise tolerance (Notes 2, 3, 4, 5, 7, 9, 10)		—	-12	—	dB
Dial tone tolerance (Notes 2, 3, 4, 5, 8, 9, 11)		—	+22	—	dB
Call progress					
Lower frequency (@ -25 dBm) accept	f_{LA}	—	320	—	Hz
Upper frequency (@ -25 dBm) accept	f_{HA}	—	510	—	Hz
Lower frequency (@ -25 dBm) reject	f_{LR}	—	290	—	Hz
Upper frequency (@ -25 dBm) reject	f_{HR}	—	540	—	Hz
Receive timing					
Tone present detect time	t_{DP}	5	11	14	ms
Tone absent detect time	t_{DA}	0.5	4	8.5	ms
Tone duration accept (ref. Figure 12)	t_{REC}	—	—	40	ms
Tone duration reject (ref. Figure 12)	$t_{\overline{REC}}$	20	—	—	ms
Interdigit pause accept (ref. Figure 12)	t_{ID}	—	—	40	ms
Interdigit pause reject (ref. Figure 12)	t_{DO}	20	—	—	ms
Delay St to b3	t_{PStb3}	—	13	—	µs
Delay St to RX_O—RX_3	t_{PStRX}	—	8	—	µs
Transmit timing					
Tone burst duration (DTMF mode)	t_{BST}	50	—	52	ms
Tone pause duration (DTMF mode)	t_{PS}	50	—	52	ms
Tone burst duration (extended, call progress mode)	t_{BSTE}	100	—	104	ms
Tone pause duration (extended, call progress mode)	t_{PSE}	100	—	104	ms
Tone output					
High group output level (R_L = 10 kΩ)	V_{HOUT}	-6.1	—	-2.1	dBm
Low group output level (R_L = 10 kΩ)	V_{LOUT}	-8.1	—	-4.1	dBm
Pre-emphasis (R_L = 10 kΩ)	dB_P	0	2	3	dB
Output distortion (R_L = 10 kΩ, 3.4 kHz bandwidth)	THD	—	-25	—	dB
Frequency deviation (f = 3.5795 MHz)	f_D	—	± 0.7	± 1.5	%
Output load resistance	R_{LT}	10	—	50	kΩ
Microprocessor interface					
ϕ 2 cycle period	t_{CYC}	0.5	—	—	µs
ϕ2 high pulse width	t_{CH}	200	—	—	ns
ϕ2 low pulse width	t_{CL}	180	—		ns
ϕ2 rise and fall time	t_R, t_F	—	—	25	ns
Address, R/$\overline{W}$ hold time	t_{AH}, t_{RWH}	10	—	—	ns
Address, R/$\overline{W}$ setup time (prior to ϕ2)	t_{AS}, t_{RWS}	23	—	—	ns

Table 12 AC Characteristics (continued)

Parameter	Symbol	Min	Typ*	Max	Units
Microprocessor interface (continued)					
Data hold time (read)	t_{DHR}	22	—	—	ns
ϕ2 to valid data delay (read) (200 pF load)	t_{DDR}	—	—	150	ns
Data setup time (write)	t_{DSW}	45	—	—	ns
Data hold time (write)	t_{DHW}	10	—	—	ns
Input capacitance, D0—D3	C_{IN}	—	5	—	pF
Output capacitance, $\overline{IRQ}$/CP	$C/_{OUT}$	—	5	—	pF
DTMF clock					
Crystal clock frequency	f_C	3.5759	3.5795	3.5831	MHz
Clock input rise time (external clock)	t_{LHCL}	—	—	110	ns
Clock input fall time (external clock)	t_{HLCL}	—	—	110	ns
Clock input duty cycle (external clock)	DC_{CL}	40	50	60	%
Capacitive load, OSC2	C_{LO}	—	—	30	pF

All voltages referenced to unless otherwise noted. V_{DD} = 5.0 V ± 5%; V_{SS} = 0 V; f_C = 3.579545 MHz; T_A = -40°C to +85°C
*Typical values are for use as design aids only, and are not guaranteed or subject to production testing.

Notes:
1. dBm = decibels above or below a reference power of 1 mW into a 600 Ω load.
2. Digit sequence consists of all 16 DTMF tones.
3. Tone duration = 40 ms. Tone pause = 40 ms.
4. Nominal DTMF frequencies are used.
5. Both tones in the composite signal have an equal amplitude.
6. The tone pair is deviated by ± 1.5% ± 2 Hz.
7. Bandwidth limited (3 kHz) Gaussian noise.
8. The precise dial tone frequencies are 350 and 440 Hz (± 2%).
9. For an error rate of less than 1 in 10,000.
10. Referenced to the lowest amplitude tone in the DTMF signal.
11. Referenced to the minimum valid accept level.

Table 13 Electrical Characteristics - Gain Setting Amplifier

Parameter	Symbol	Min	Typ*	Max	Units
Input leakage current ($V_{SS} \le V_{IN} \le V_{DD}$)	I_{IN}	—	100	—	nA
Input resistance	R_{IN}	—	10	—	MΩ
Input offset voltage	V_{OS}	—	25	—	mV
Power supply rejection (1 KHz)	PSRR	—	60	—	dB
Common mode rejection (-3.0 V ≤ $\mathbf{V}_{IN}$ ≤ 3.0 V)	CMRR	—	60	—	dB
DC open-loop voltage gain	A_{VOL}	—	65	—	dB
Unity gain bandwidth	BW	—	1.5	—	MHz
Output voltage swing ($R_L \ge$ 100 KΩ to V_{SS})	V_O	—	4.5	—	V_{PP}
Maximum capacitive load, GS	C_L	—	100	—	pF
Maximum resistive load, GS	R_L	—	50	—	KΩ
Common mode range (no load)	V_{CM}	—	3.0	—	V_{PP}

All voltages referenced to unless otherwise noted. V_{DD} = 5.0 V; V_{SS} = 0 V; T_A = 25°C
*Typical values are for use as design aids only, and are not guaranteed or subject to production testing.

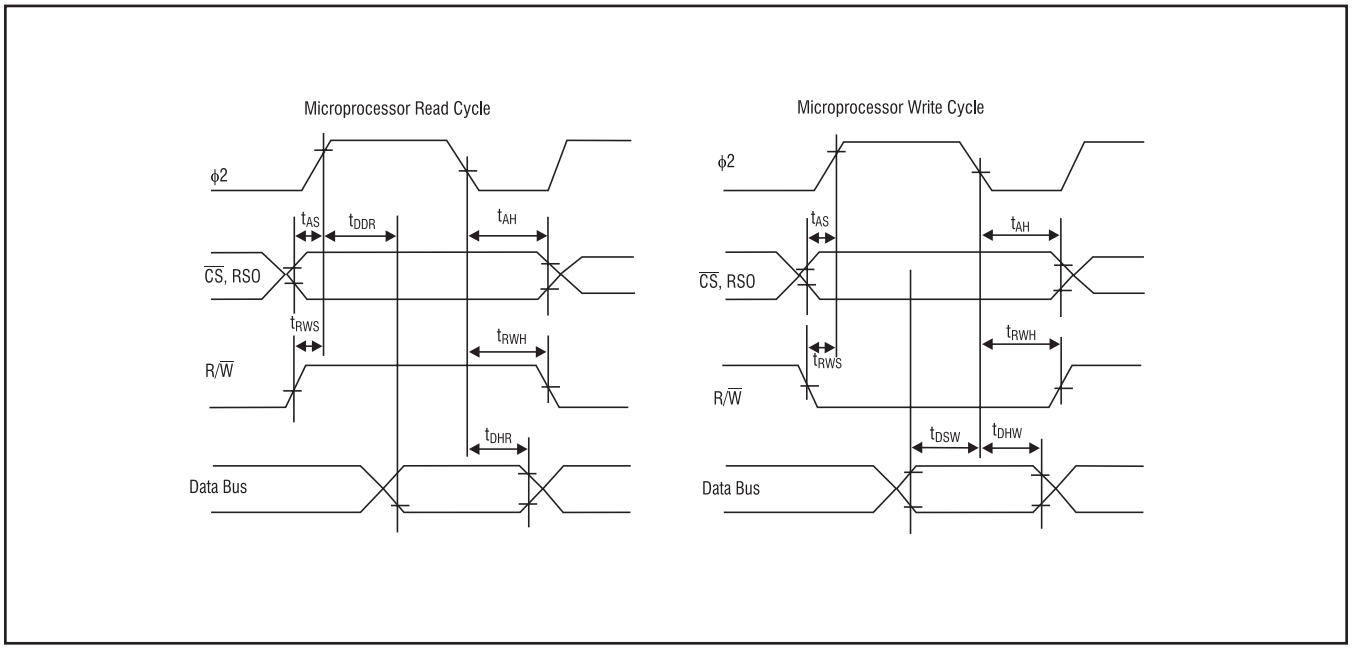


Figure 11 Timing Diagrams

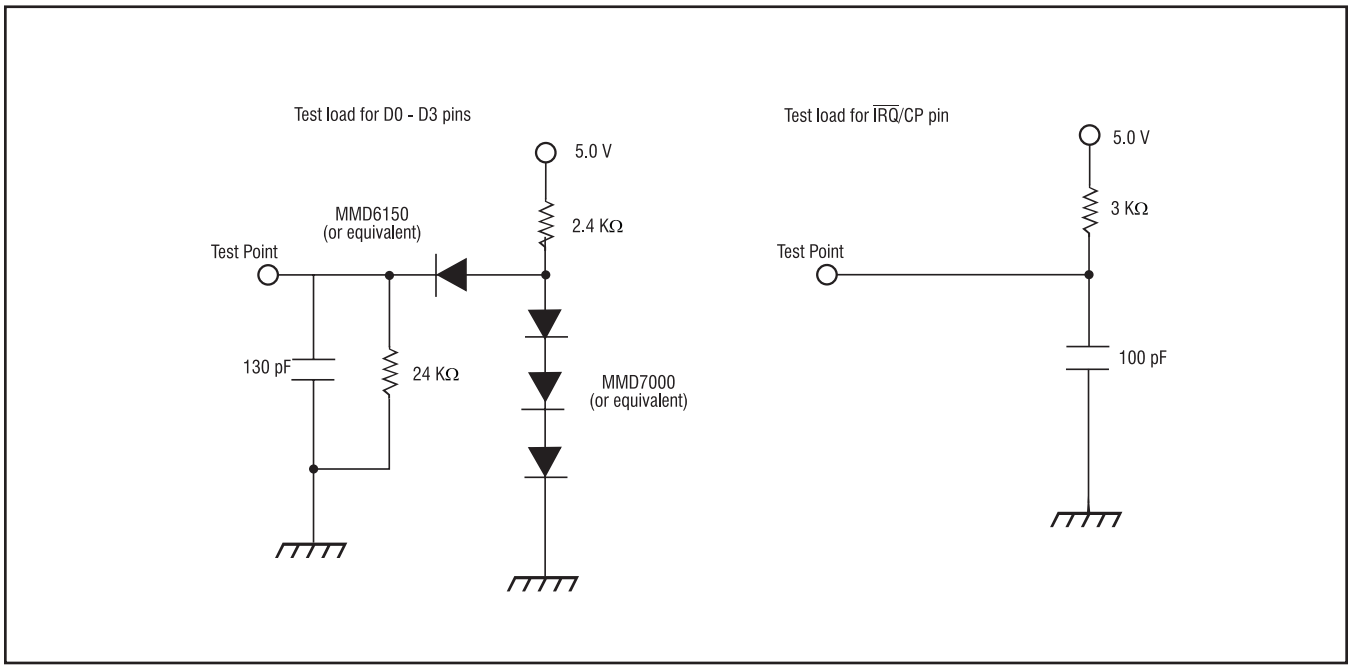
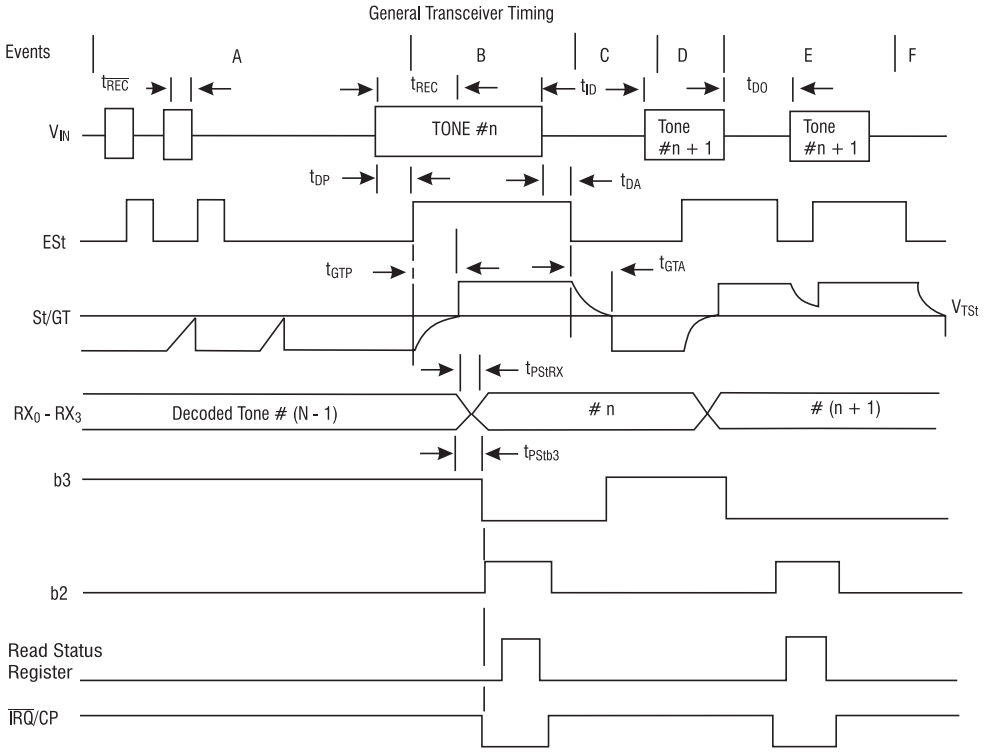


Figure 12 Test Loads



Explanation of Events

(A) Tone bursts detected, tone duration invalid, RX Data Register not updated.

(B) Tone #n detected, tone duration valid, tone decoded and latched in RX Data Register.

(C) End of tone #n detected, tone absent duration valid, RX Data Register remain latched until next valid tone.

(D) Tone #n + 1 detected, tone duration valid, tone decoded and latched in RX Data Register.

(E) Acceptable dropout of tone #n + 1, tone absent duration invalid, RX Data Register remain latched.

(F) End of tone #n + 1 detected, tone absent duration valid, RX Data Register remain latched until next valid tone.

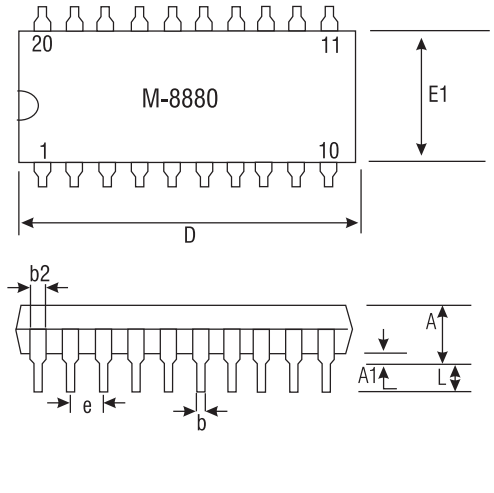
Explanation of Symbols

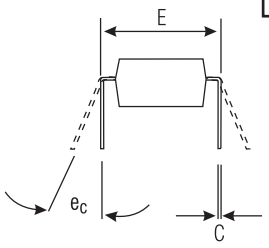
V_{IN}	DTMF composite input signal.
ESt	Early steering output. Indicates detection of valid tone frequencies.
St/GT	Steering input/guard time output. Drives external RC timing circuit.
RX_0-RX_3	4-bit decoded data in receive data register.
b3	Delayed steering output. Indicates that valid frequencies have been present/absent for the required guard time, thus constituting a valid DTMF signal.
b2	Output enable (input). A low level shifts Q1 - Q4 to its high impedance state.
$\overline{IRQ}$/CP	Interrupt is active indicating that new data is in the RX data register. The interrupt is cleared after the status register is ready.
$t_{\overline{REC}}$	Maximum DTMF signal duration not detected as valid.
t_{REC}	Minimum DTMF signal duration required for valid recognition.
t_{ID}	Minimum time between valid DTMF signals.
t_{DO}	Maximum allowable dropout during valid DTMF signal.
t_{DP}	Time to detect the presence of valid DTMF signals.
t_{DA}	Time to detect the absence of valid DTMF signals.
T_{GTP}	Guard time, tone present.
t_{GTA}	Guard time, tone absent.

Figure 13 Timing Diagrams

Drawing not to scale.
Does not reflect actual part marking.

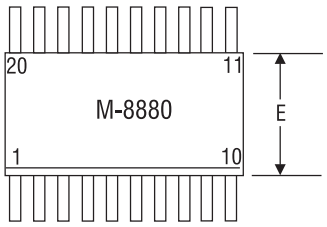
20-Pin DIP

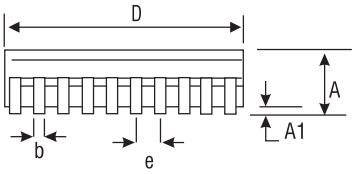


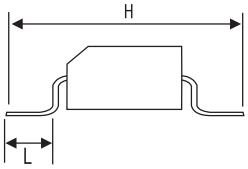


Tolerances				
	Inches		Metric (mm)	
	Min	Max	Min	Max
A		.210		5.33
A1	.015		.38	
b	.014	.022	.36	.56
b_2	.045	.070	1.14	1.78
C	.008	.014	.20	.36
D	.980	1.060	24.89	26.92
E	.300	.325	7.62	8.26
E1	.240	.280	6.10	7.11
e	.100 BSC		2.54 BSC	
e_C	0°	15°	0°	15°
L	.115	.150	2.92	3.81

20-Pin SOIC







Tolerances				
	Inches		Metric (mm)	
	Min	Max	Min	Max
A	.093	.104	2.35	2.65
A1	.004	.012	.10	.30
b	.013	.020	.33	.51
D	.496	.512	12.60	13.00
E	.291	.299	7.39	7.59
e	.050 BSC		1.27 BSC	
H	.394	.419	10.00	10.65
L	.016	.050	.40	1.27

Figure 14 Package Dimensions

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